REMARKS

Applicants appreciate the USPTO's thorough review of the present application, and respectfully request reconsideration in light of the preceding amendments and the following remarks.

Claim 22 has been amended to better define the claimed invention. No new matter has been introduced through the foregoing amendments.

The **new matter objection** to the previous Amendment is respectfully traversed as to both form and substance.

As to form, a new matter objection is proper only if the specification is amended to include the alleged new matter. In this case, the specification was not amended; rather, claim 26 was amended to include the alleged new matter. Thus, the new matter objection is improper.

As to substance, Applicants respectfully submit that previously amended claim 26 includes no new matter. The USPTO's position is that the "only capacitor" feature added to claim 26 constitutes new matter because there is nothing in the original disclosure that clearly indicates the added feature. Applicants respectfully disagree, because claim 26 finds *explicit* support in FIG. 1 as filed which discloses the "only capacitor" feature at 32 or 34. Applicants further submit that the disclosure, as cited in the Office Action, is sufficiently broad to cover (i) the species where there is only one capacitor connected to the associated connection and (ii) the species where there are more than one capacitors connected to the connection. Claim 26 was not drafted to cover both species. Rather, claim 26 is directed specifically to the species (i) and is positively supported by the original disclosure as detailed above.

For each of the reasons detailed above, Applicants respectfully submit the new matter objection is improper and should be withdrawn.

The ***35 U.S.C. 112, second paragraph* rejection** of claim 22 is noted. Applicants

respectfully disagree with the USPTO's position, because a person of ordinary skill in the art would understand the meaning of "immediately" in light of the original disclosure. Notwithstanding and solely for the purpose of expediting prosecution, claim 22 has been amended to remove the alleged indefiniteness issues. Claim 22 now recites, among other things, "upon the second transition between the second and first intervals: turning off, without any capacitive delay, the path of the second transistor while maintaining, during said second transition and during an initial portion of the first interval, the path of the first transistor off by changing the second voltage from the second value to the first value while the second capacitor remains switched off and the first capacitor is charged."

Amended claim 22 finds solid support in the application as filed, especially FIGs. 1, 2 and the corresponding text at paragraph 0032 of the *published* application. In particular, the specification discloses that the second capacitor 54/34 is switched off in the waveform portion 78 on FIG. 2. Thus, when the transition 80 occurs, the second capacitor 54/34 is still switched off. Refer to FIG. 1, since the second capacitor 54/34 remains switched off when the transition 80 occurs, there is no capacitor coupled to the link 30, and hence, the inverted signal from inverter 30 reaches the gate of NFET 50 without any capacitive delay, as now presently claimed.

Withdrawal of the *35 U.S.C. 112, second paragraph* rejection is believed appropriate and therefore respectfully requested.

The art rejections are respectfully traversed for the reasons presented in the previous Amendment(s) which are incorporated by reference herein for the sake of simplicity. Applicants will nevertheless proceed with their remarks.

As to **the rejections relying on *Naganuma* and *Bui***, Applicants respectfully disagree with the USPTO's position that it would have been obvious to connect the *Bui* capacitors 807 and 808 separately [1] to different nodes b) and c) of *Naganuma*. *Bui* expressly requires that the capacitors

[1] *See* Office Action at page 6, lines 4-5 from bottom.

807 and 808 be commonly connected to the same node as best seen in FIG. 8A of the reference. The rejection, therefore, lacks a clear articulation [2] of the reason(s) why it would have been obvious to separate the commonly connected capacitors 807, 808 of *Bui*.

In addition, Applicants respectfully maintain the position detailed in the previous Amendment that a person of ordinary skill in the art would have been motivated, if at all, only to connect both capacitors 807, 808 of *Bui* to the same node of *Naganuma* as exemplified in the previously presented *Exhibit A*. Such a combination, if at all proper, would fail to teach or suggest the "only capacitor" features of independent claims 26 and 31. The combination, if at all proper, would also fail to teach or suggest the "without any capacitive delay" feature of independent claim 22 since at least one of capacitors 807, 808 must remain ON when a transition occurs, thereby capacitively delaying the switching off of the respective transistor 71, 72 of *Naganuma*.

Withdrawal of the *35 U.S.C. 103(a)* rejection relying on *Naganuma* and *Bui* as well as the *35 U.S.C. 103(a)* rejection relying on *Naganuma*, *Bui* and *Yoshizawa*, is believed appropriate and therefore respectfully requested.

As to the **rejections relying on *Naganuma* and *Love***, Applicants respectfully disagree with the USPTO's position that it would have been obvious to combine *Naganuma* with *Love*. The reason is that the delay element of *Love*, i.e., capacitor 80, is provided between two inverter stages, 78, 90,[3] i.e., within an inverter. The *Love* reference does not supply any teaching or suggestion of providing a delay stage after or downstream of the inverter. *Naganuma* discloses an inverter at 51, 52. A person of ordinary skill in the art learning of the teachings of *Naganuma* and *Love* would have included, if at all, the *Love* delay stage within the *Naganuma* inverter 51, 52, rather than downstream thereof as proposed in the Office Action.

In addition, the Office Action's proposed combination, if at all proper, would include a

[2] Rejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *KSR International Co. v. Teleflex Inc.*, 550 U.S. at ___, 82 USPQ2d at 1396.

NMOS capacitor where a PMOS capacitor is required, and *vice versa*.[4] The USPTO's proposed combination would still be different from the claimed invention as admitted in the Office Action. It is unclear from the language of the Office Action as to why it would have been obvious to *further* modify the NMOS capacitor imported from *Love* into a PMOS capacitor to arrive, if at all, at the claimed invention. The USPTO's obviousness rationale, due to this missing step, is unconvincing and should be withdrawn.

Finally, the NMOS v. PMOS difference is not a minor one, contrary to the USPTO's position.[5] It should be noted that NMOS capacitor 80 of *Love* is provided to limit the rising speed of the signal at node 76. The reference also discloses how to limit the falling speed of the signal at node 76, by moving the resistor 72 to the branch associated with transistor 70, and apparently, by additionally changing the capacitor 80 to a PMOS.[6] Thus, *Love* clearly discloses that the polarity of capacitor 80 cannot be arbitrarily set; rather, the reference requires that the polarity of capacitor 80 must be specifically chosen to provide appropriate rising/falling speed limiting action.[7] Given the above overall teaching of *Love*, a person of ordinary skill in the art, if at all motivated, would have combined *Naganuma* and *Love* in the exact manner exemplarily depicted in the previously presented *Exhibit B*, with a NMOS capacitor 80, instead of a PMOS capacitor. The person of ordinary skill in the art would not have been motivated to further change the NMOS to a PMOS, because as detailed in footnote 7 herein, such further modification would fail to limit the rising speed at the output c) of the *Naganuma* inverter, and hence, would defeat the intended purpose of inserting the *Love* capacitor 80 into the *Naganuma* circuit.

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[3] *See Love* at column 3 lines 54-55, and 59-60.
[4] *See* Office Action at page 20, line 5.
[5] *Id.*
[6] *See Love* at column 6 lines 40-44 and the paragraph bridging columns 6-7.
[7] For example, a person of ordinary skill in the art would understand that if in the configuration shown in FIG. 3 of *Love* capacitor 80 is changed to a PMOS, capacitor 80 will no longer provide the required rising speed limiting action. The reason is that as the signal at node 79 rises, a PMOS capacitor 80 will be switched off without limiting the rising speed of the signal at node 76.

For each of the reasons detailed above, Applicants respectfully submit the art rejections relying on *Naganuma* and *Love* are improper and should be withdrawn.

Each of the Examiner's rejections has been traversed. Accordingly, Applicants respectfully submit that all claims are now in condition for allowance. Early and favorable indication of allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 08-2025 and please credit any excess fees to such deposit account.

Respectfully submitted,

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